

FIGURE 1A

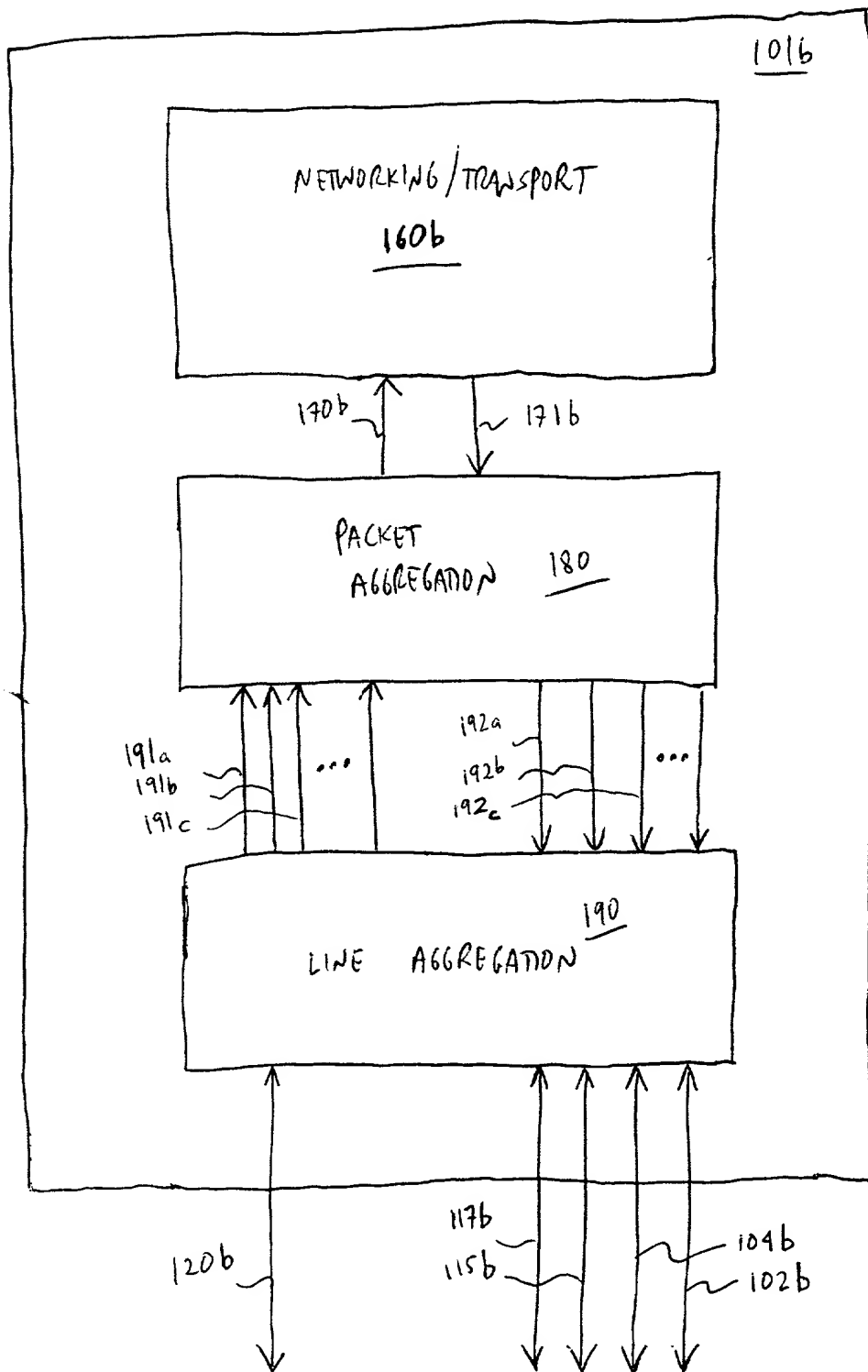


FIGURE 1B

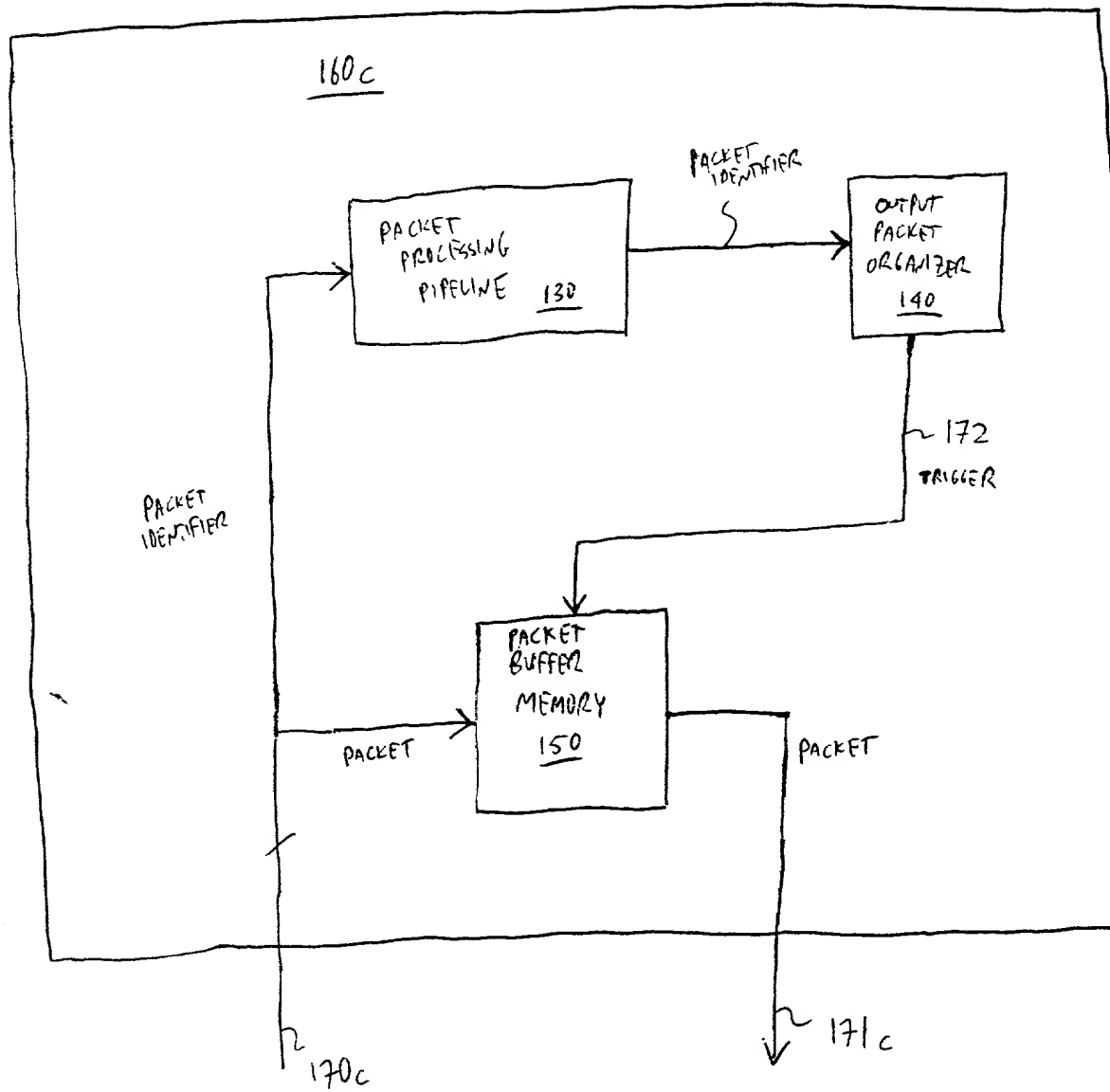


FIGURE 1c

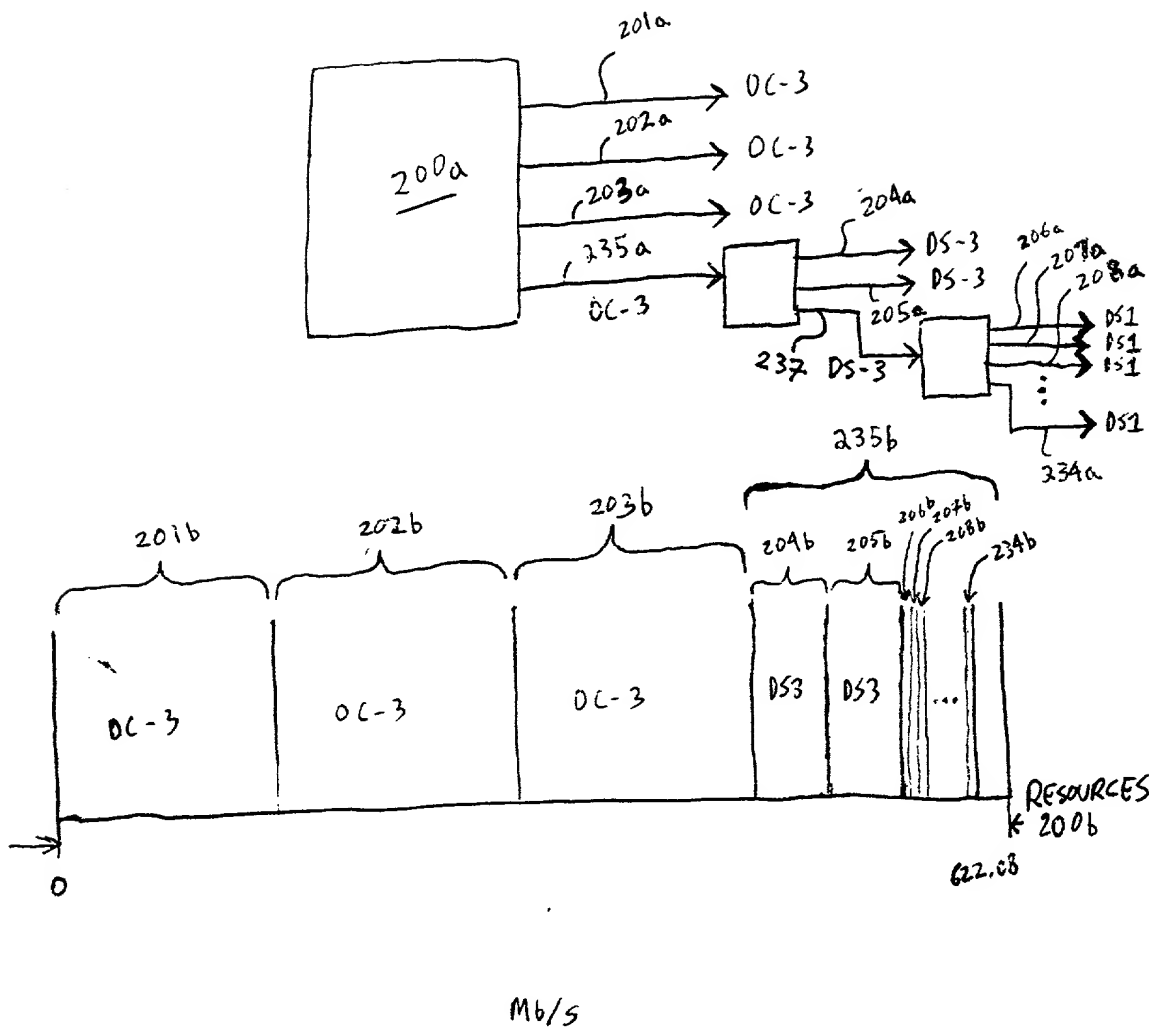


FIGURE 2

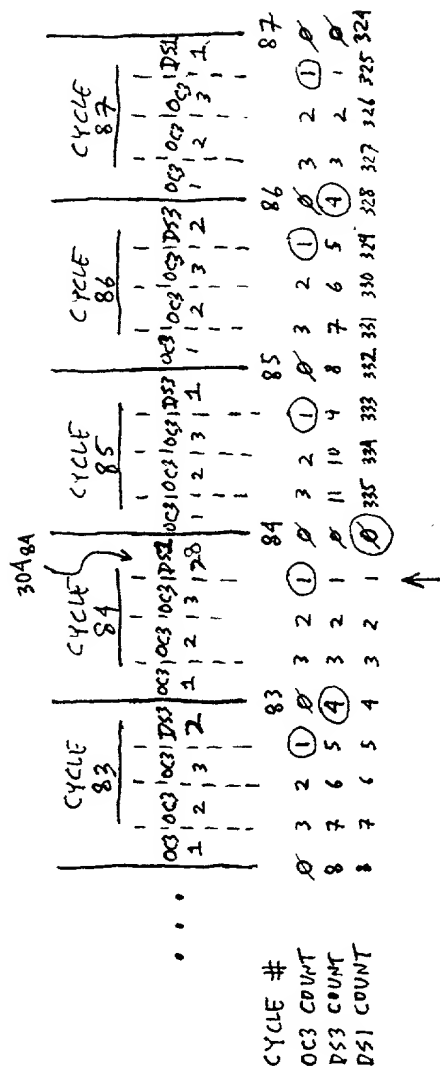
Cycle #	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6	Cycle 7	Cycle 8
OC3 COUNT	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303
DS3 COUNT	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303
DS1 COUNT	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303	302, 301, 304, 303

OC3 circle "not completed"

DS3 circle "not completed"

OC3 circle "completed"

DS3 circle "completed"



⊗ = done bit received

FIGURE 3

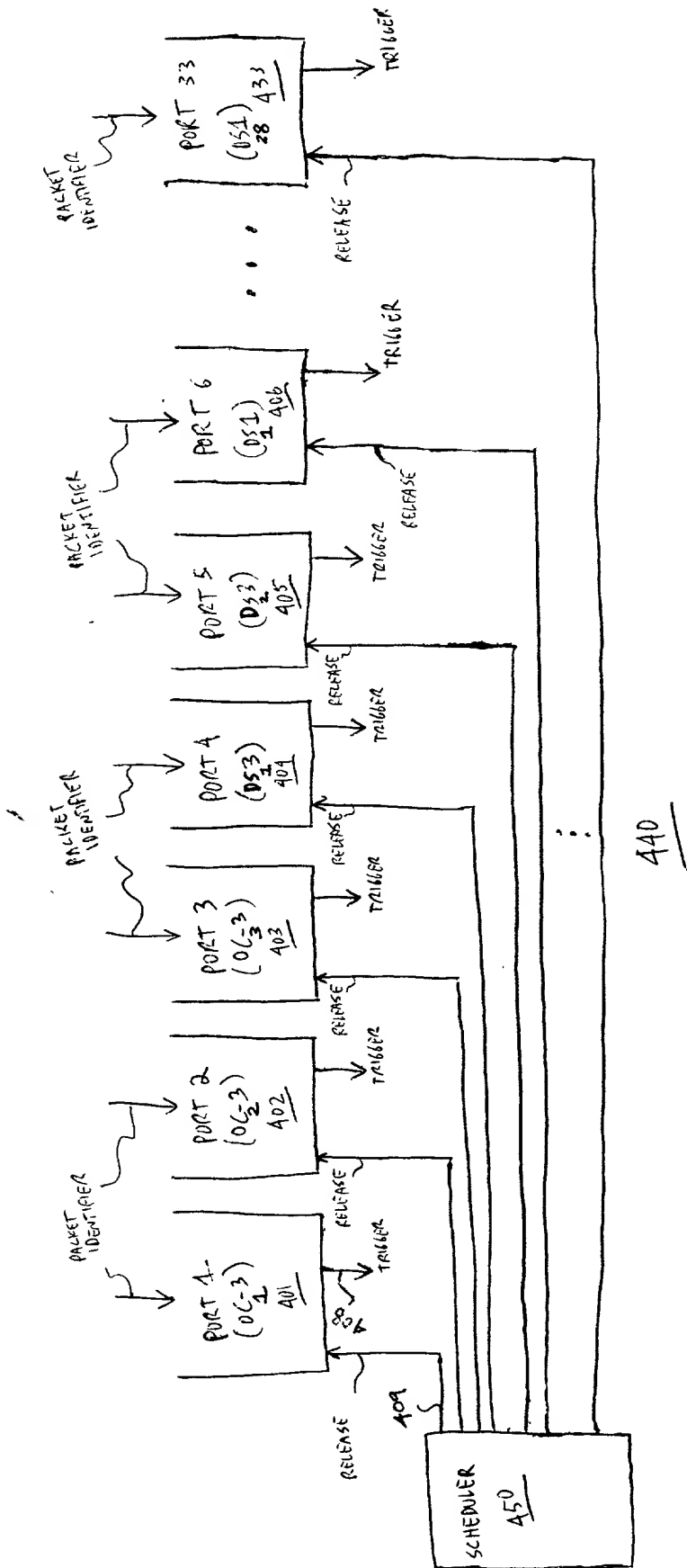


FIGURE 4

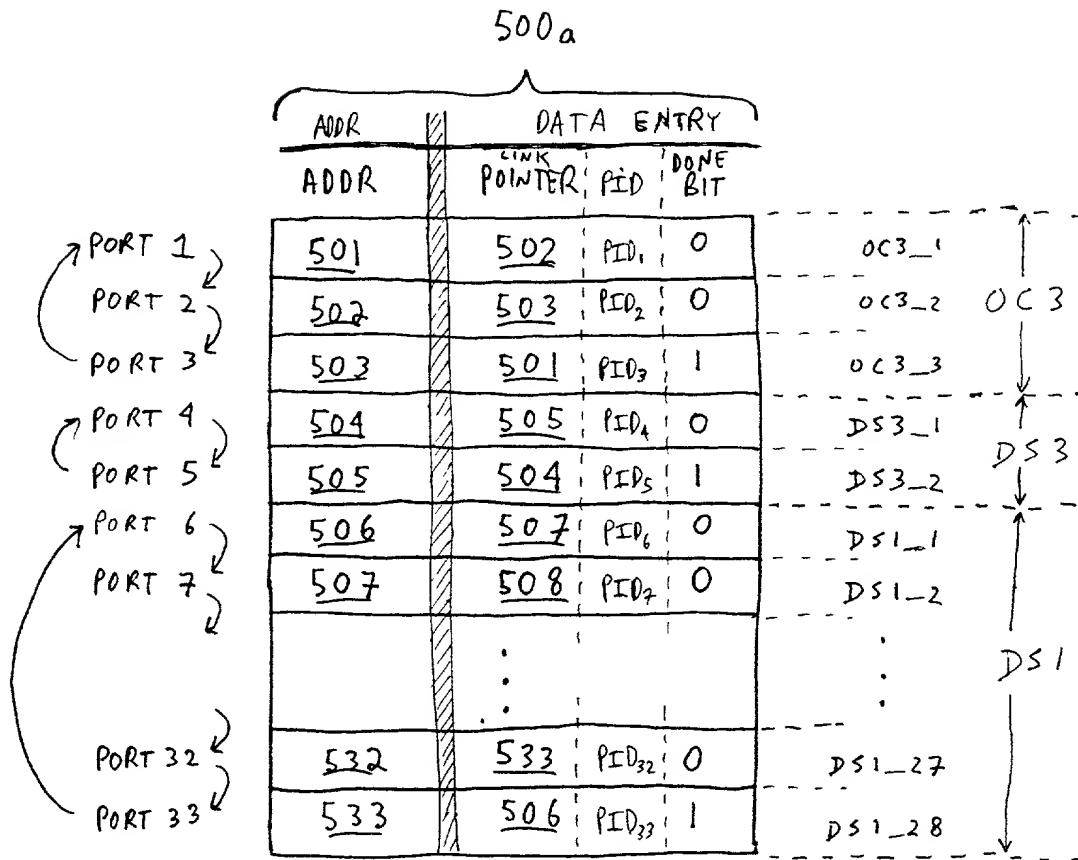


FIG. 5A

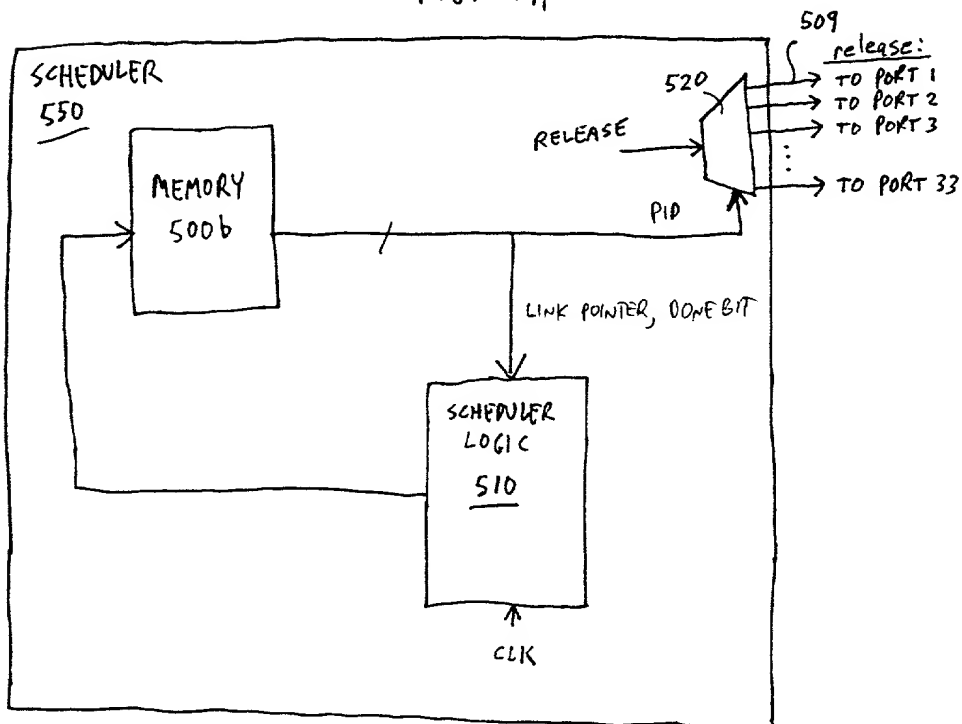


FIG. 5B

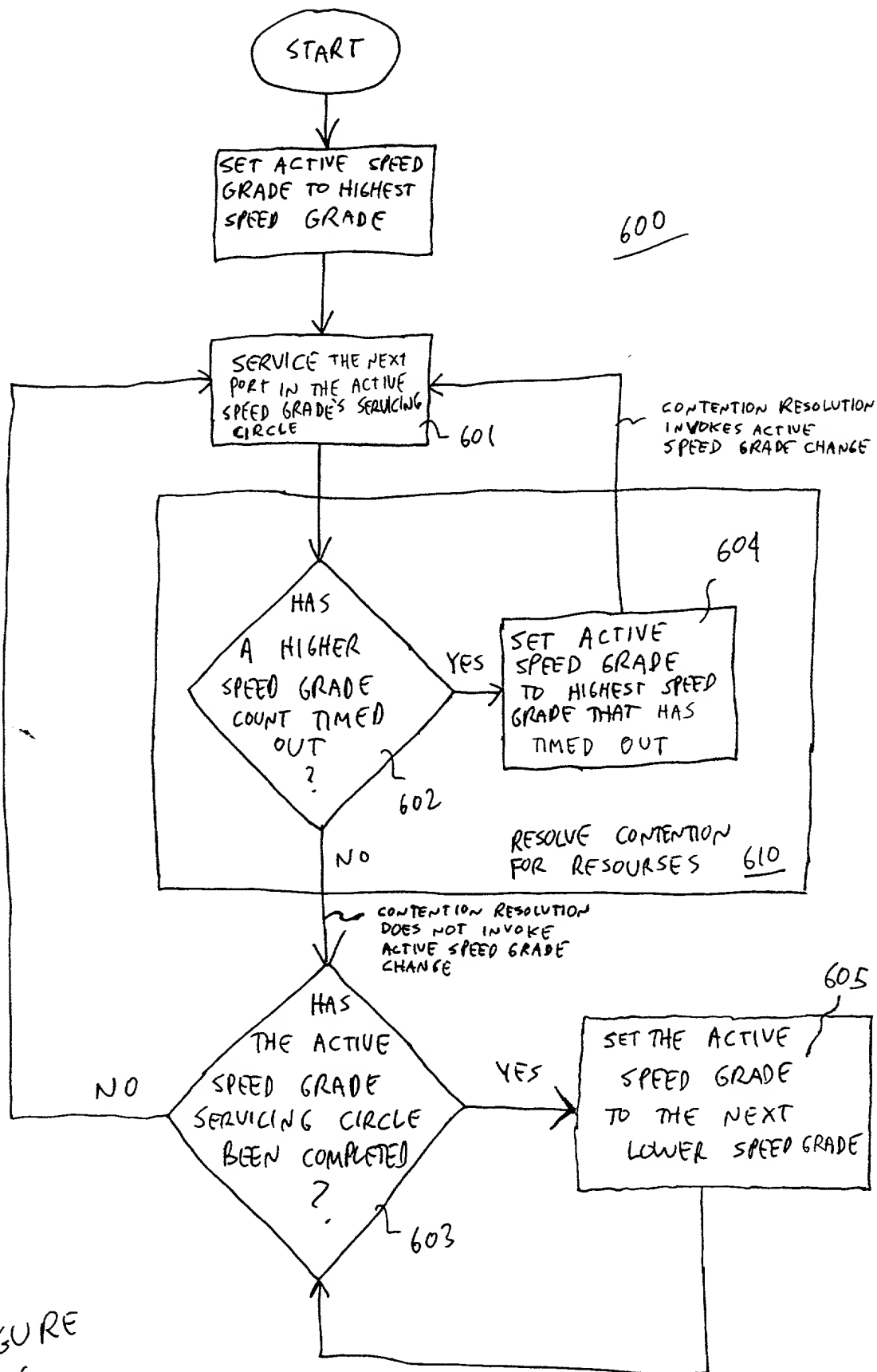


FIGURE
6

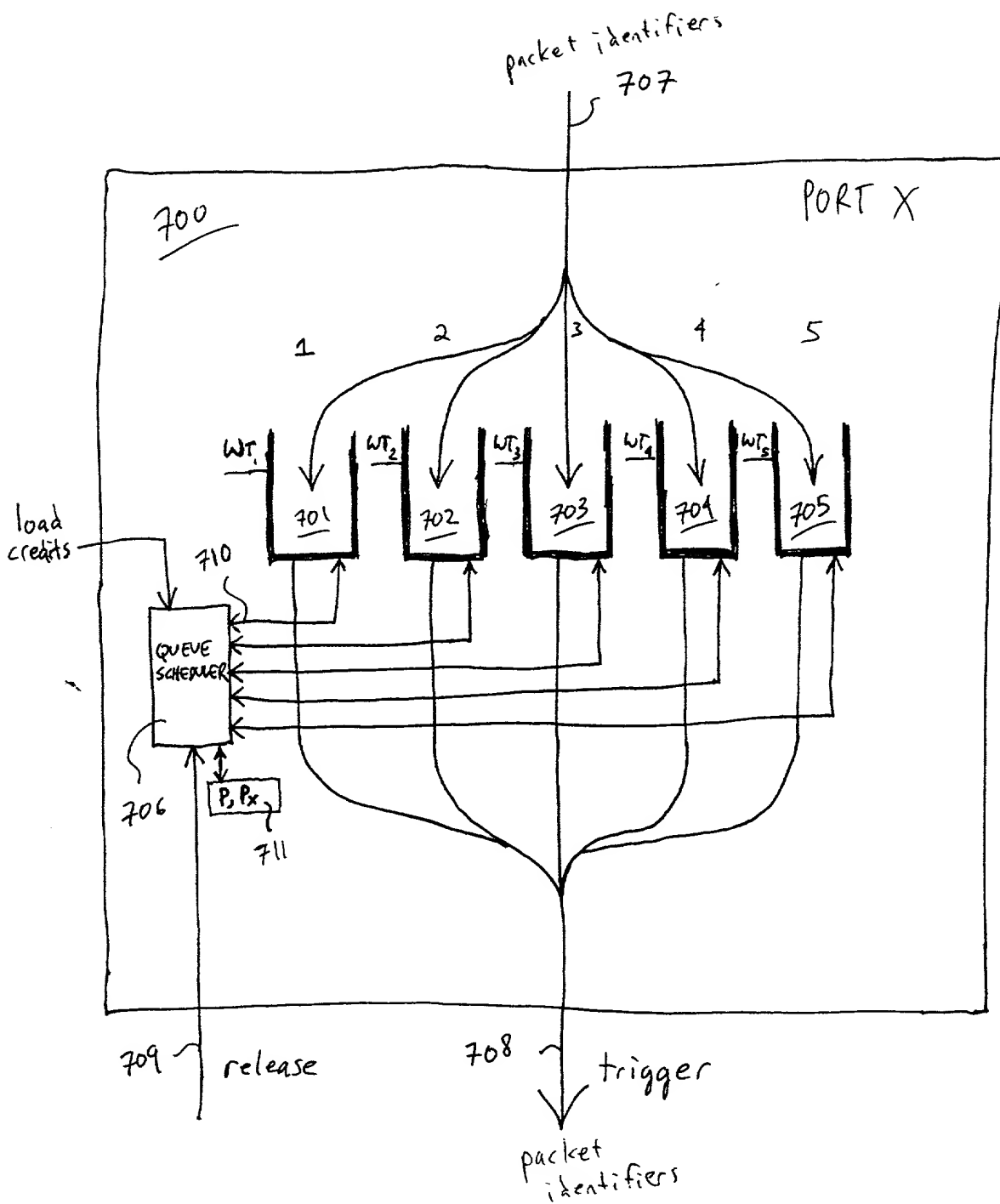
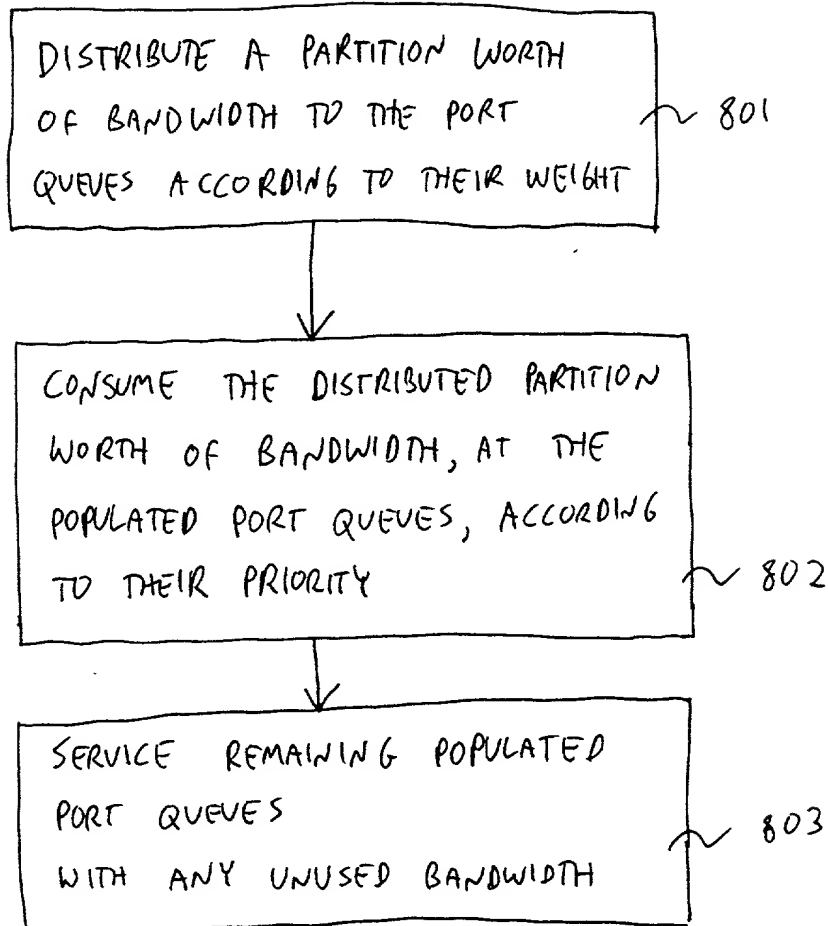


FIGURE 7



800

FIGURE 8

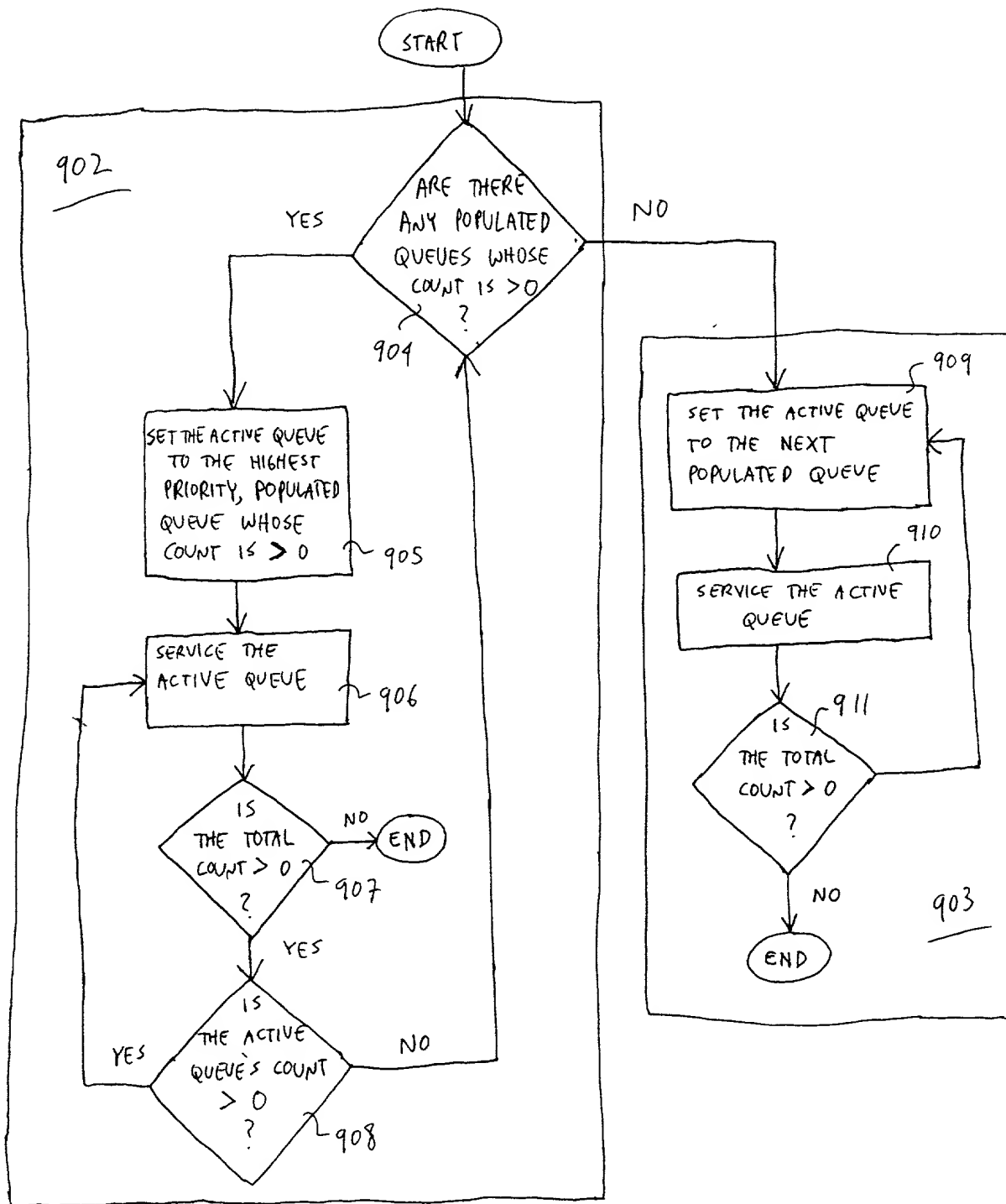


FIGURE 9